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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,666	09/30/2003	Randy B. Osborne	42P16964	8981

7590 08/12/2008
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EXAMINER

BATAILLE, PIERRE MICHEL

ART UNIT	PAPER NUMBER
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2186

MAIL DATE	DELIVERY MODE
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08/12/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RANDY B. OSBORNE

Appeal 2008-0335
Application 10/676,666
Technology Center 2100

Decided: August 12, 2008

Before JAMES D. THOMAS, HOWARD B. BLANKENSHIP,
And ST. JOHN COURTENAY III, *Administrative Patent Judges*.
THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1 through 15. We have jurisdiction under 35 U.S.C. § 6(b).

As best representative of the disclosed and claimed invention,
independent claim 1 is reproduced below:

1. An apparatus comprising:

a plurality of banks, each bank comprised of a plurality of memory cells organized into an array of rows and columns, wherein only one row of memory cells in each bank may be activated to be open to be accessed at any given time;

control logic coupled to the plurality of banks to control accesses made to each bank in response to commands received from an external device including a precharge command wherein banks of the plurality of banks that are affected by the precharge command are individually specified; and

a plurality of signal lines coupling the control logic to the external device able to support the precharge command using individual ones of a subset of the plurality of signal lines to individually specify the banks of the plurality of banks that are affected by the precharge command.

The following references are relied on by the Examiner:

Watanabe	US 5,463,590	Oct. 31, 1995
Shaver	US 5,974,501	Oct. 26, 1999
Rovati	US 6,182,192 B1	Jan. 30, 2001

Appellant's Admitted Prior Art.

"NEC Preliminary User's Manual, Memory Controller NA85E535, NBA85E535Vxx," Oct. 2002.

Claims 14 and 15 stand rejected under the enablement provision of 35 U.S.C. § 112. All claims on appeal, claims 1 through 15, also stand rejected under 35 U.S.C. § 103. As evidence of obviousness as to claims 1 through 5, the Examiner relies upon Watanabe in view of Appellant's Admitted Prior Art (APA) in a first stated rejection. To this initial

combination of references in the second stated rejection, the Examiner adds NEC as to claims 6 through 9 and 11 through 13. To this second stated rejection, the Examiner further adds Rovati as to claim 10 in a third stated rejection. Lastly, in a fourth stated rejection, the Examiner rejects claims 14 and 15 as being obvious over the combination of Watanabe in view of APA and NEC, further in view of Shaver.

Rather than repeat the positions of the Appellant and the Examiner, reference is made to the Brief (no Reply Brief has been filed) for Appellant's positions, and to the Answer for the Examiner's positions.

OPINION

We turn first to the rejection of claims 14 and 15 under the enablement provision of the first paragraph of 35 U.S.C. § 112. As to the enablement issue, the Specification of the patent must teach those skilled in the art how to make and use the claimed invention without undue experimentation. *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997). This same case indicates that the scope of the claims must bear a reasonable correlation to the scope of enablement provided by the disclosure. Enablement is also not precluded even if some experimentation is necessary, although the amount of experimentation needed must not be unduly excessive. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384 (Fed. Cir. 1986).

Briefly, the Examiner takes the position that the testing capability within the first clause of independent claim 14 is not sufficiently detailed in the Specification such as to require undue experimentation to make and use the presently claimed invention. Among Appellant's arguments as to this rejection at pages 5 through 7 of the Brief, Appellant takes the position that the Examiner has not set forth a reasonable basis to question the adequacy of the disclosure to conclude that undue experimentation would have been necessary to make and use the claimed invention. The Examiner's responsive view at page 8 of the Answer recognizes what Appellant is claiming but urges that the disclosure is silent on exactly "how" the subject matter of the testing clause may be achieved. The Examiner also takes the view that there is an absence of any explicit teachings as to the testing clauses such that the Examiner considers that it would require undue experimentation to make and use the claimed invention.

We reverse this rejection. Beginning with the discussion at the bottom of page 21 in paragraph [0031] in the original filed Specification, the discussion of the computer system in 400 in figure 4 makes mention of the CPU carrying out various tests on the memory device 490 in this figure to determine what type DRAM memory device element 490 is. Since independent claim 14 includes limitations discussed in subsequent paragraphs and shown in flow chart figure 5 and flow chart figure 6 through the discussion at the top of page 23 in paragraph [0033], we conclude that the artisan would require only some or a reasonable amount of experimentation to make and use the claimed features argued by the Examiner to be deficient. Therefore, the position of the Examiner rejecting

claims 14 and 15 as lacking proper basis within the enablement provision of the first paragraph of 35 U.S.C. § 112 is reversed.

On the other hand, we sustain the first stated rejection under 35 U.S.C. § 103, that of claims 1 through 5, as being obvious over Watanabe in view APA. As the Examiner has reasoned the rejection at pages 3 through 5 of the Answer and the Responsive Arguments at pages 8 and 9 of the Answer, the Examiner appears to rely on Watanabe as representative of prior art multi-bank memory elements comprised of plural memory cells organized in a conventional manner. Watanabe appears to be consistent with what Appellant recognizes as prior art memory devices at originally filed Specification page 9, paragraphs 13 through 14, as illustrated in figure 1 of the disclosed invention as well as the corresponding discussion in Specification page 20 and 21 in paragraph [0029].

Appellant's corresponding arguments at pages 7 through 10 in the Brief take the initial position that the Examiner's apparent reliance upon the discussion in originally filed Specification page 13, lines 16 through 19, which comprise subject matter in paragraph [0020] at page 4 of the Answer, is not prior art. We agree. On the other hand, the discussion in the paragraph bridging pages 8 and 9 of the Answer clarifies the Examiner's position and makes reference to the background section of the present application, particularly the discussion in paragraph [0002] at pages 2 and 3 of the original Specification as filed, as the basis of the rejection.

The Examiner's reliance upon this discussion at paragraph [0002] quotes that it "has also become common practice to attempt to reduce both costs and the physical size of DRAM devices by multiplexing multiple

functions onto the various signal input and outputs.” The Examiner’s reasoning appears to rely upon this capability of multiplexing multiple functions onto various, or otherwise selective, as claimed, subsets of conventional signal lines, as the basis to reject the present independent claim 1 on appeal. The bulk of this paragraph makes reference to the conventionality of multiplexing in the art. Moreover, the remaining parts of the background of the invention at Specification pages 1 through 4 are equally pertinent. Of particular mention is the discussion in original filed Specification page 4 in paragraph [0004] that the desire in the art has been the acceptance of the ability of commands with a given format to access a very limited portion of a DRAM memory device that may be specified in a particular command structure. The end result is the ability to transmit multiple commands to cover a portion of such a device that is less than all of the device.

Thus, in conjunction with the Examiner’s reasoning at pages 4 and 9 of the Answer, we agree with the Examiner’s conclusion that it would have been obvious for the artisan to utilize less than the whole plurality of available signal lines, such as the subset of them as claimed, to have caused the selection of a specified memory bank portion based upon externally controlled commands in lieu of those conventional in the art that are taught by Wanatabe alone. The Examiner’s conclusion is fully consistent with the Appellant’s APA and the trends in the art as stated. Thus, the rejection of claims 1 to 5 is sustained.

Lastly, we address as a group the separately stated rejections of claims 6 through 9 and 11 through 13, the separate rejection of claim 10 and the separate rejection of claims 14 and 15. Each of the independent claims associated in these rejections (claims 6, 9, and 14) recite in some manner the requirement to electrically close an open row within the memory device. It is this limitation common to these independent claims and their respective dependent claims that the Examiner has not addressed in the statement of the rejection of these claims and in the responsive arguments of the Answer as well. As such, the Examiner has not pointed to any teachings or suggestions in Watanabe and Appellant's APA to support a conclusion of obviousness of this noted feature. The same may be said of Rovati and Shaver. This noted feature common among the independent claims 6, 9, and 14 has been argued by Appellant as to the respective rejections beginning with the discussion at page 10 of the principal Brief. Therefore, on the basis of the weight of the arguments and evidence before us and in view of the absence of the Examiner addressing this common limitation, we must reverse the rejections of claims 6 through 15.

In summary we have reversed the rejection of claims 14 and 15 under the first paragraph of 35 U.S.C. § 112. On the one hand, while we have sustained the rejection of claims 1 through 5 under 35 U.S.C. § 103, we have reversed the rejection of claims 6 through 15 on this statutory basis. As such, the decision of the Examiner is affirmed in part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. §1.136(a). See 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

pgc

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